GANE140-700BBA

700 V, 140 mOhm Gallium Nitride (GaN) FET in DPAK package

13 March 2025 **Product data sheet**

1. General description

The GANE140-700DBA is a general purpose 700 V, 140 mΩ Gallium Nitride (GaN) FET in a DPAK package. It is a normally-off e-mode device offering superior performance.

2. Features and benefits

- Enhancement mode - normally-off power switch
- Ultra high frequency switching capability
- No body diode
- Low gate charge, low output charge
- Qualified for standard applications
- ESD protection
- RoHS, Pb-free, REACH-compliant
- High efficiency and high power density

3. Applications

- High power density and high efficiency power conversion
- AC-to-DC converters, totem pole PFC
- DC-to-DC converters
- Fast battery charging, mobile phone, laptop, tablet and USB type-C chargers
- Datacom and telecom (AC-to-DC and DC-to-DC) converters
- Motor drives
- Solar (PV) inverters
- Class D audio amplifiers, TV PSU and LED drivers

4. Quick reference data

Table 1. Quick reference data

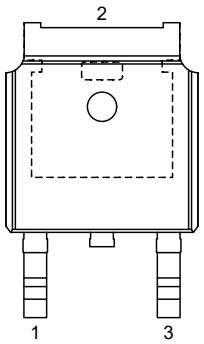
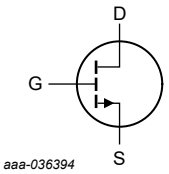
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 150 °C		-	-	700	V
V_{TDS}	transient drain to source voltage	t_p < 200 µs	[1]	-	-	800	V
I_D	drain current	V_{GS} = 6 V; T_{mb} = 25 °C; Fig. 2	[2]	-	-	17	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	110	W
T_j	junction temperature			-55	-	150	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 6 V; I_D = 5 A; T_j = 25 °C; Fig. 12; Fig. 13; Fig. 14		-	106	140	mΩ
		V_{GS} = 6 V; I_D = 5 A; T_j = 150 °C; Fig. 12; Fig. 15		-	230	-	mΩ
R_G	gate resistance	f = 5 MHz; T_j = 25 °C; open drain		-	5.3	-	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 5 A; V_{DS} = 400 V; V_{GS} = 6 V; T_j = 25 °C; Fig. 16; Fig. 17		-	1.2	-	nC
$Q_{G(tot)}$	total gate charge			-	3.5	-	nC
Q_{oss}	output charge	V_{GS} = 0 V; 0 V ≤ V_{DS} ≤ 400 V; T_j = 25 °C; Fig. 22	[3]	-	33	-	nC

[1] Intended for non-repetitive events
[2] Limited by device saturation
[3] Q_r is not specified separately from Q_{oss} for e-mode GaN FETs, since $Q_r = Q_{oss} + Q_D$, and $Q_D = 0$. (Q_D is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q_{oss} have to be transferred for e-mode GaN FETs.)

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 TO252 (SOT428-2)	
2	S	souce		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GANE140-700BBA	TO252	plastic, single-ended surface-mounted package (DPAK); 3 leads; 2.286 mm pitch; 6.1 mm x 6.6 mm x 2.3 mm body	SOT428-2

7. Marking

Table 4. Marking codes

Type number	Marking code
GANE140-700BBA	140SBBA

8. Limiting values

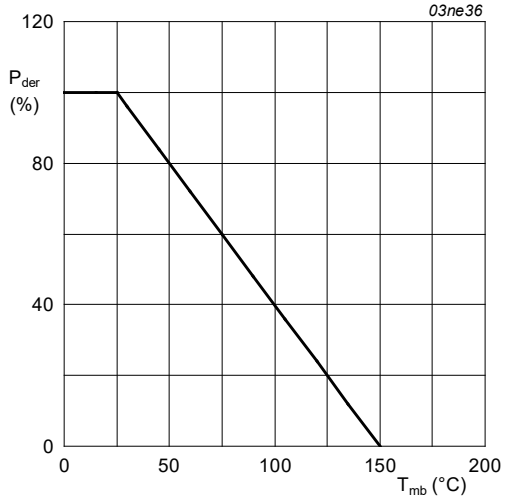
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 150 °C		-	700	V

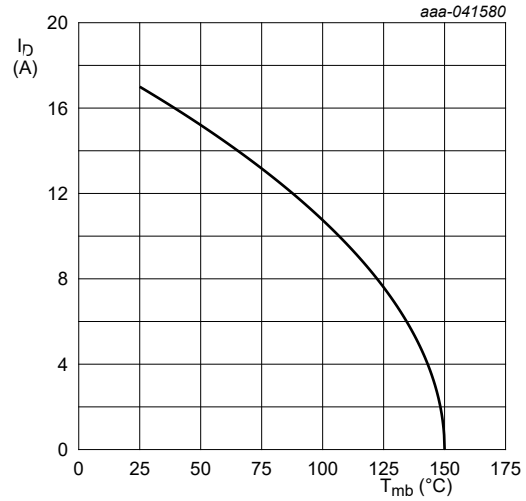
Symbol	Parameter	Conditions		Min	Max	Unit
V_{TDS}	transient drain to source voltage	t_p < 200 µs	[1]	-	800	V
V_{GS}	gate-source voltage		[2]	-6	7	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	110	W
I_D	drain current	V_{GS} = 6 V; T_{mb} = 25 °C; Fig. 2	[3]	-	17	A
I_{DM}	peak drain current	pulsed; t_p = 10 µs; T_{mb} = 25 °C; Fig. 3	[4]	-	32	A
		pulsed; t_p = 10 µs; T_{mb} = 125 °C; Fig. 4	[4]	-	18	A
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C

[1] Intended for non-repetitive events
[2] The minimum V_{GS} is clamped by ESD protection circuit
[3] Limited by device saturation
[4] Limit was extracted from characterization test, not measured during production



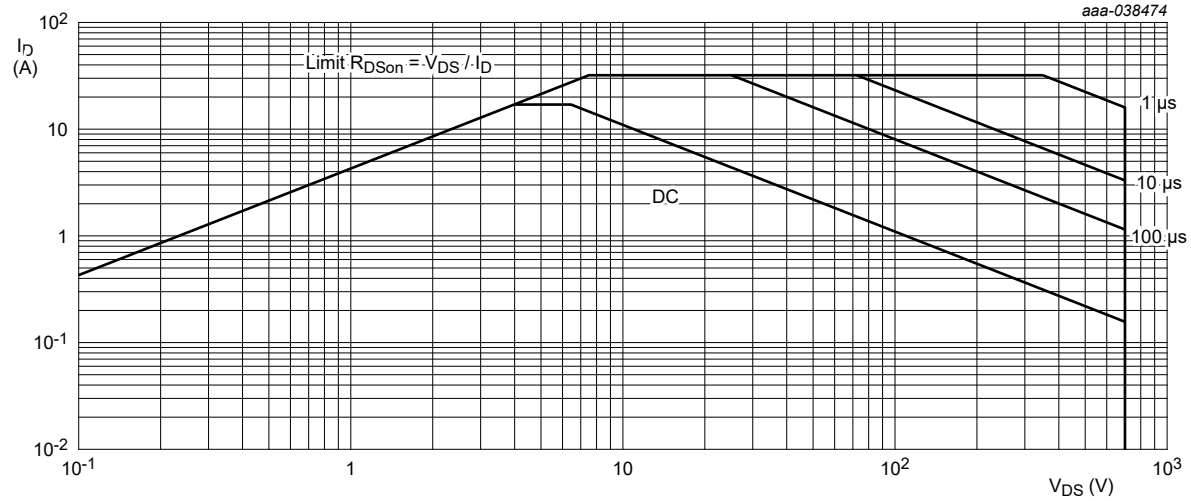
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



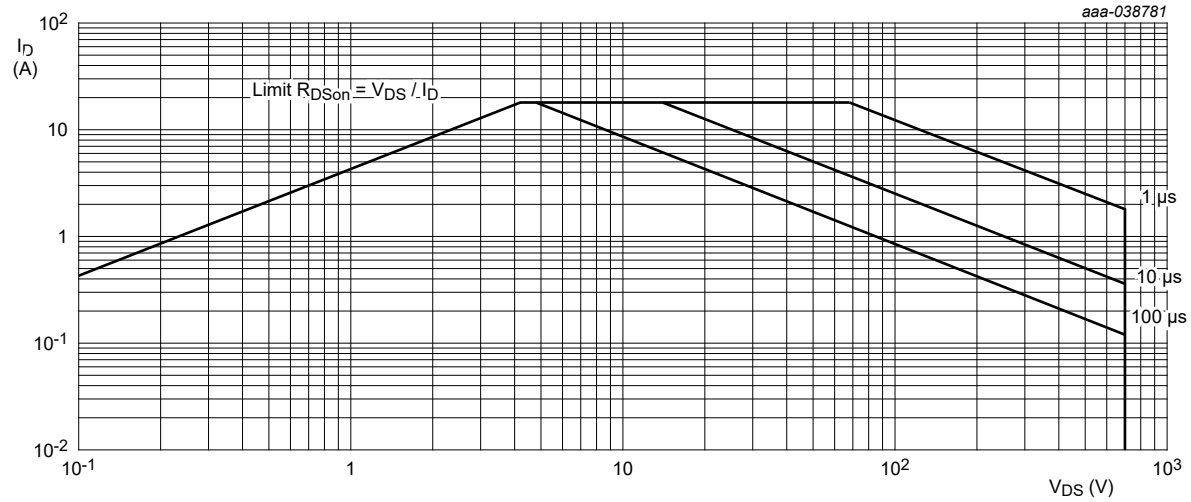
$V_{GS} \geq 6$ V

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



T_{mb} = 125 °C; I_{DM} is a single pulse

Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	-	1.14	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	-	53	K/W

[1] $R_{th(j-a)}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

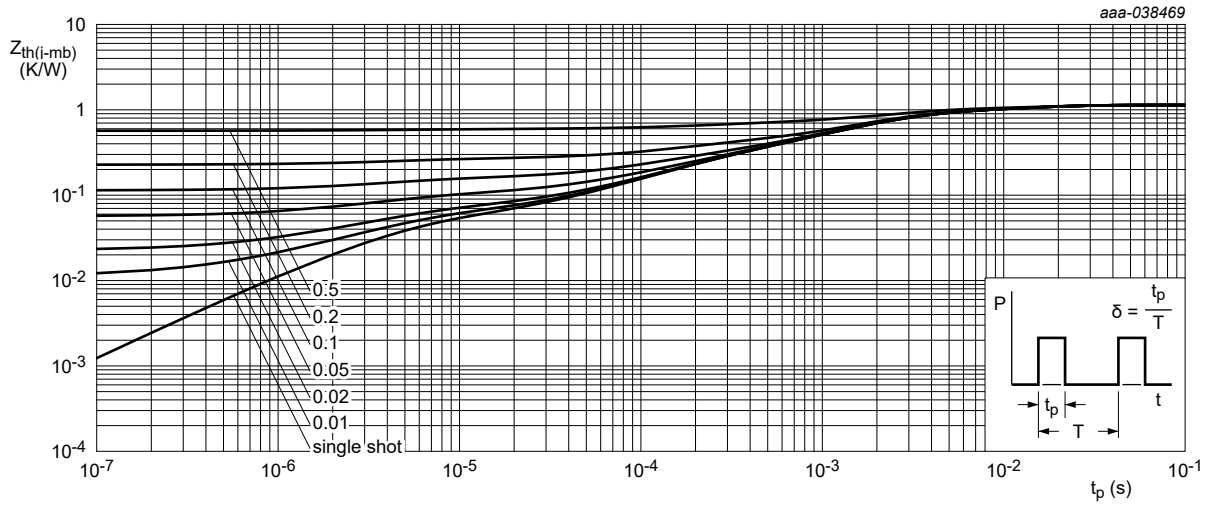


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

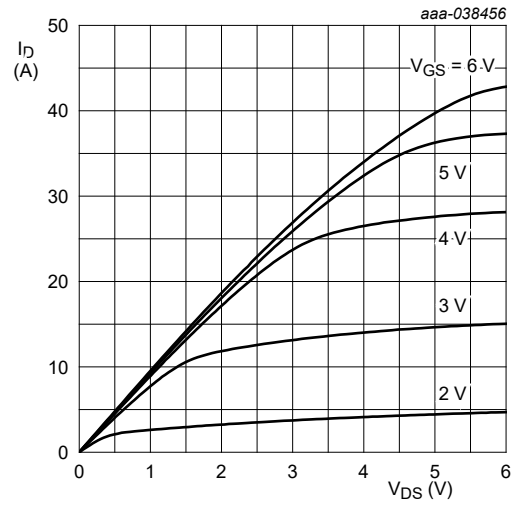
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{GS(th)}$	gate-source threshold voltage	I_D = 17.2 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 9		1.2	1.7	2.5	V
		I_D = 17.2 mA; V_{DS}=V_{GS}; T_j = 150 °C; Fig. 9		-	1.7	-	V
I_{DSS}	drain leakage current	V_{DS} = 700 V; V_{GS} = 0 V; T_j = 25 °C; Fig. 10		-	0.6	25	µA
		V_{DS} = 700 V; V_{GS} = 0 V; T_j = 150 °C; Fig. 10		-	7	-	µA
I_{GSS}	gate leakage current	V_{GS} = 6 V; V_{DS} = 0 V; T_j = 25 °C; Fig. 11		-	70	-	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = 6 V; I_D = 5 A; T_j = 25 °C; Fig. 12; Fig. 13; Fig. 14		-	106	140	mΩ
		V_{GS} = 6 V; I_D = 5 A; T_j = 150 °C; Fig. 12; Fig. 15		-	230	-	mΩ
R_G	gate resistance	f = 5 MHz; T_j = 25 °C; open drain		-	5.3	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 5 A; V_{DS} = 400 V; V_{GS} = 6 V; T_j = 25 °C; Fig. 16; Fig. 17		-	3.5	-	nC
Q_{GS}	gate-source charge			-	0.3	-	nC
Q_{GD}	gate-drain charge			-	1.2	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 5 A; V_{DS} = 400 V; T_j = 25 °C; Fig. 17		-	2.1	-	V
C_{iss}	input capacitance	V_{DS} = 400 V; V_{GS} = 0 V; f = 100 kHz; T_j = 25 °C; Fig. 18		-	125	-	pF
C_{oss}	output capacitance			-	41	-	pF
C_{rss}	reverse transfer capacitance			-	0.4	-	pF
$C_{o(er)}$	effective output capacitance, energy related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; T_j = 25 °C; Fig. 19	[1]	-	59	-	pF

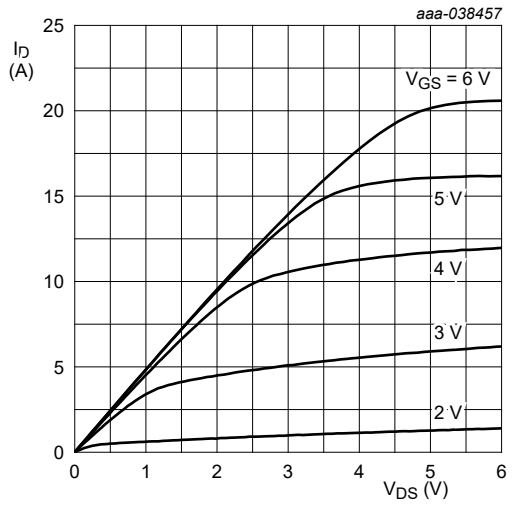
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$C_{o(tr)}$	effective output capacitance, time related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; T_j = 25 °C	[2]	-	82	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 400 V; V_{GS} = 6 V; I_D = 10 A; L = 318 µH; R_{on} = 10 Ω; R_{off} = 2 Ω; Fig. 20; Fig. 21		-	3	-	ns
t_r	rise time			-	5	-	ns
$t_{d(off)}$	turn-off delay time			-	4	-	ns
t_f	fall time			-	4	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; 0 V ≤ V_{DS} ≤ 400 V; T_j = 25 °C; Fig. 22	[3]	-	33	-	nC
Source-drain characteristics							
V_{SD}	source-drain voltage	I_S = 3.9 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 23; Fig. 24; Fig. 25; Fig. 26		-	2.4	-	V

[1] $CO_{(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V
[2] $CO_{(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V
[3] Q_r is not specified separately from Q_{oss} for e-mode GaN FETs, since $Q_r = Q_{oss} + Q_D$, and Q_D = 0. (Q_D is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q_{oss} have to be transferred for e-mode GaN FETs.)



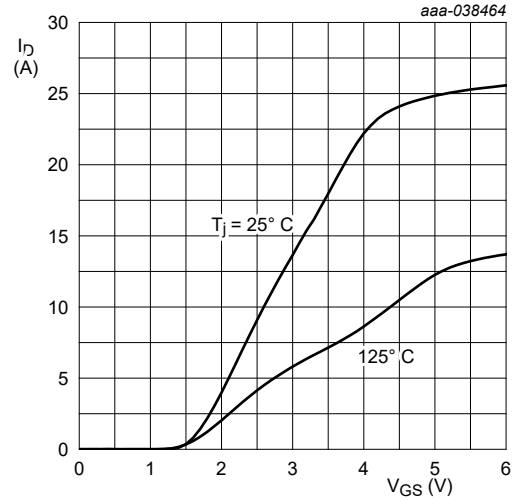
T_j = 25 °C

Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values



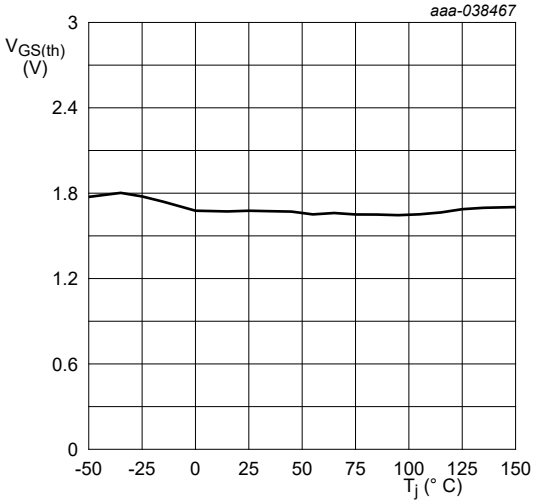
T_j = 125 °C

Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values



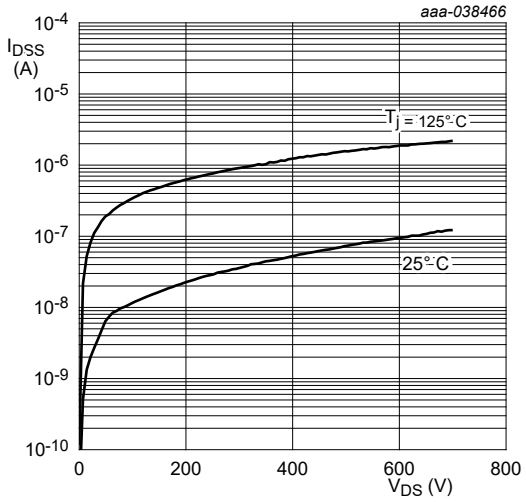
V_{DS} = 3 V

Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



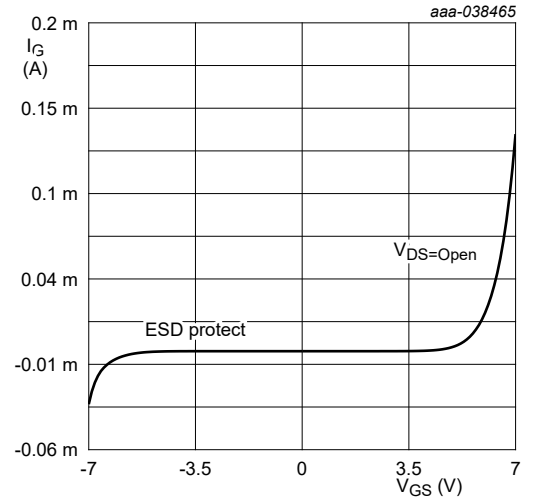
I_D = 17.2 mA ; V_{DS} = V_{GS}

Fig. 9. Gate-source threshold voltage as a function of junction temperature; typical values



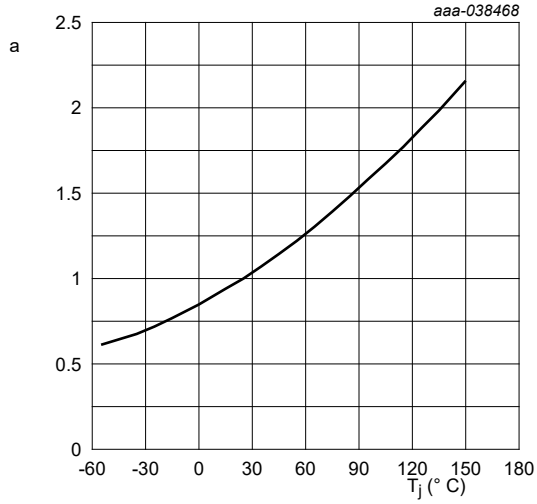
V_{GS} = 0 V

Fig. 10. Drain-source current as a function of drain-source voltage; typical values



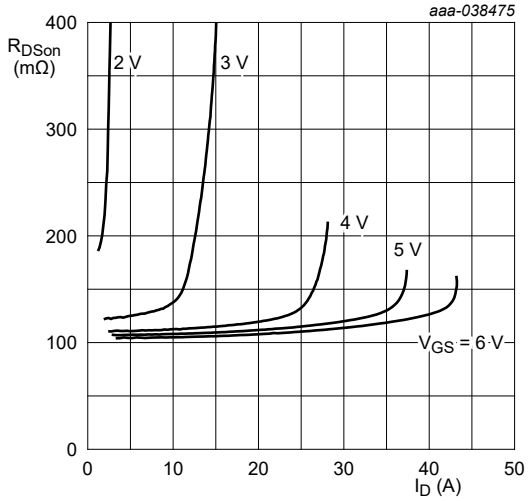
Ig reverse turn on by ESD unit

Fig. 11. Gate-source current as a function of gate-source voltage; typical values



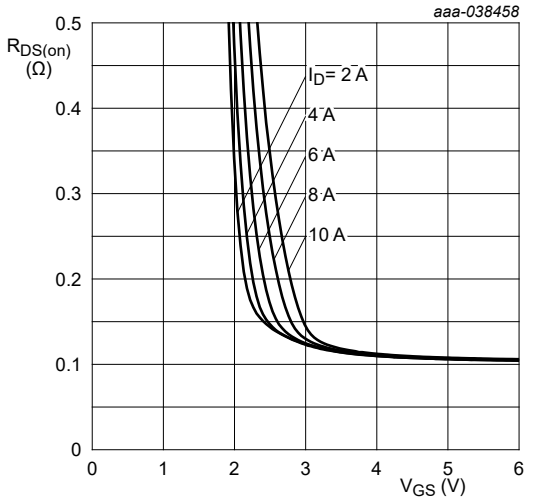
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature



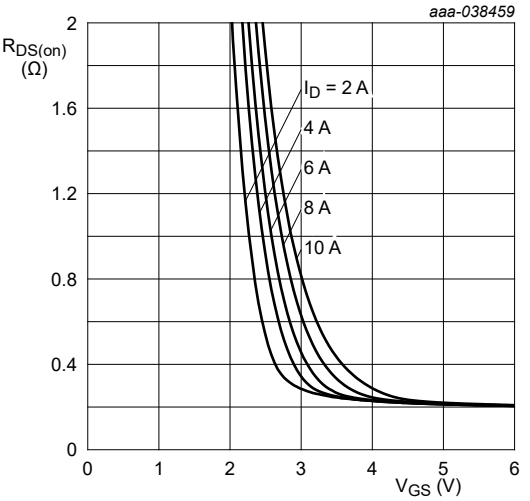
T_j = 25 °C

Fig. 13. Drain-source on-state resistance as a function of drain current ; typical values



T_j = 25 °C

Fig. 14. Drain-source on-state resistance as a function of gate-source voltage; typical values



T_j = 125 °C

Fig. 15. Drain-source on-state resistance as a function of gate-source voltage; typical values

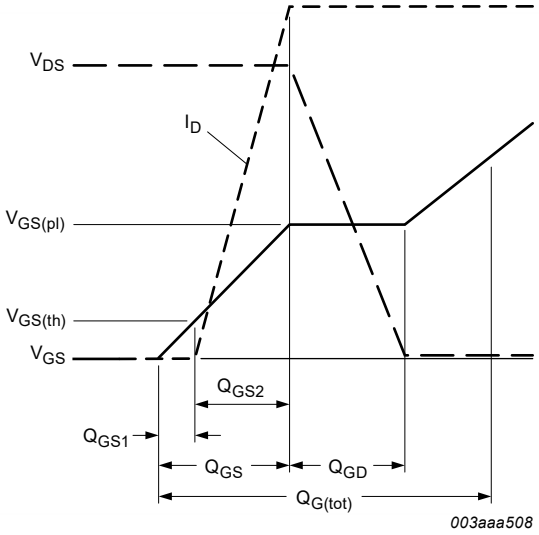
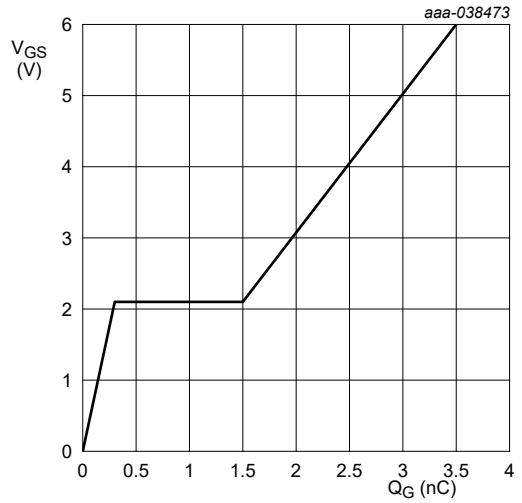
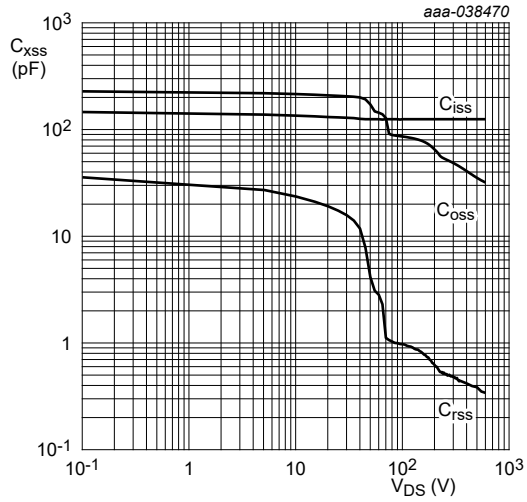


Fig. 16. Gate charge waveform definitions



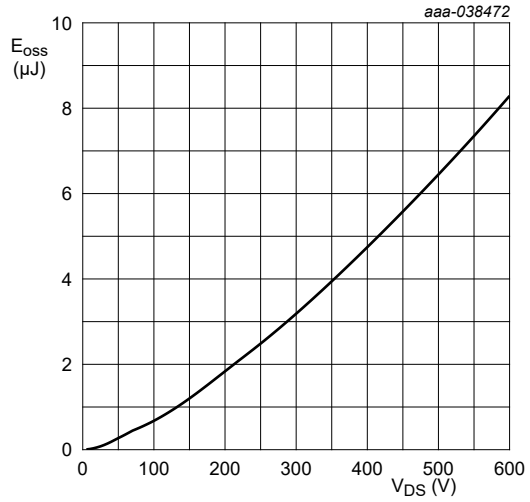
T_J = 25 °C ; I_D = 5A

Fig. 17. Gate-source voltage as a function of gate charge; typical values



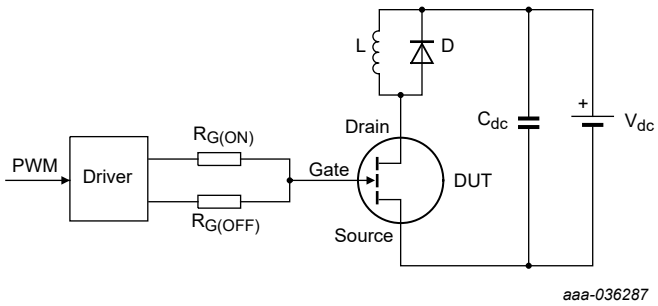
V_{GS} = 0 V; f = 100 kHz

Fig. 18. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



Freq. = 100 kHz

Fig. 19. COSS stored energy as a function of drain-source voltage; typical values



V_{DS} = 400 V; I_D = 10 A; L = 318 µH; V_{GS} = 6 V; R_{on} = 10 Ω; R_{off} = 2 Ω

Fig. 20. Switching time test circuit with inductive load

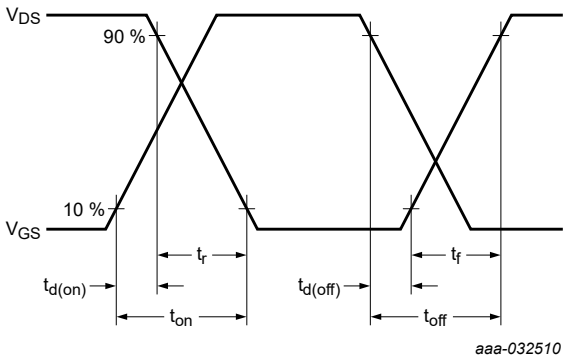
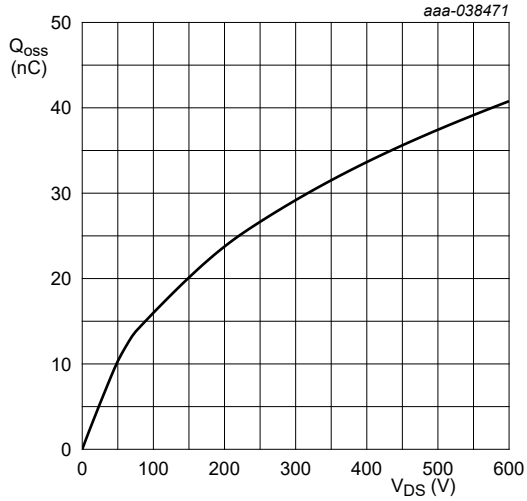
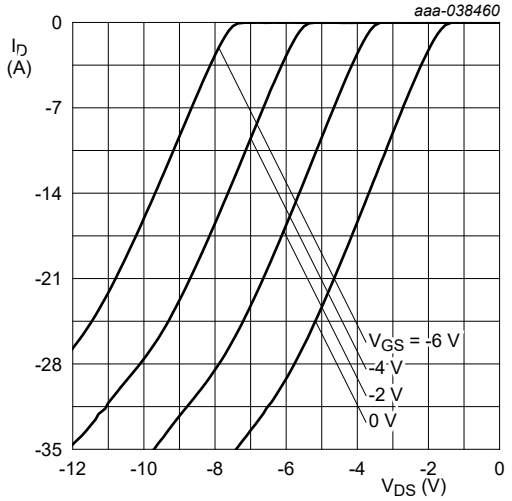


Fig. 21. Switching time waveform



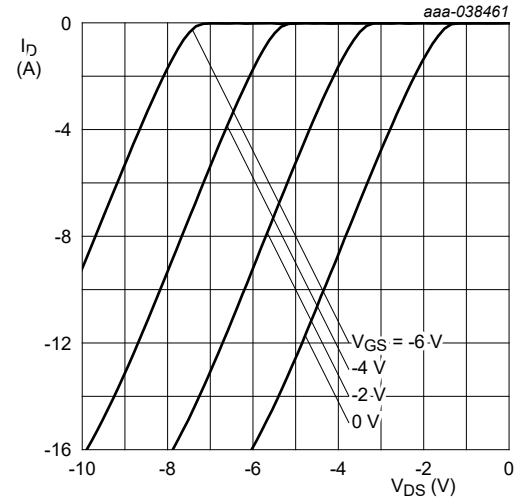
Freq. = 100 kHz

Fig. 22. Output charge as a function of drain-source voltage; typical values



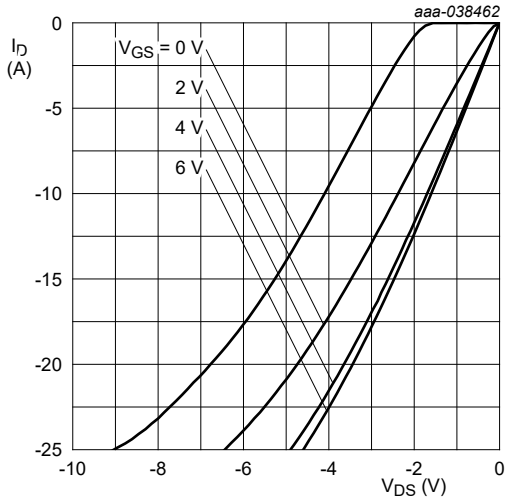
T_j = 25 °C

Fig. 23. Source current as a function of source-drain voltage; typical values



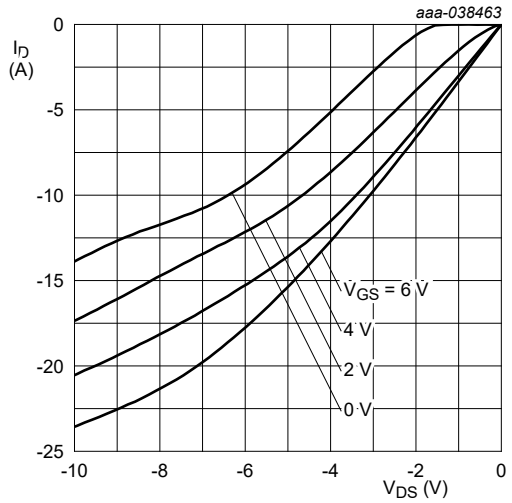
T_j = 125 °C

Fig. 24. Source current as a function of source-drain voltage; typical values



T_j = 25 °C

Fig. 25. Source current as a function of source-drain voltage; typical values

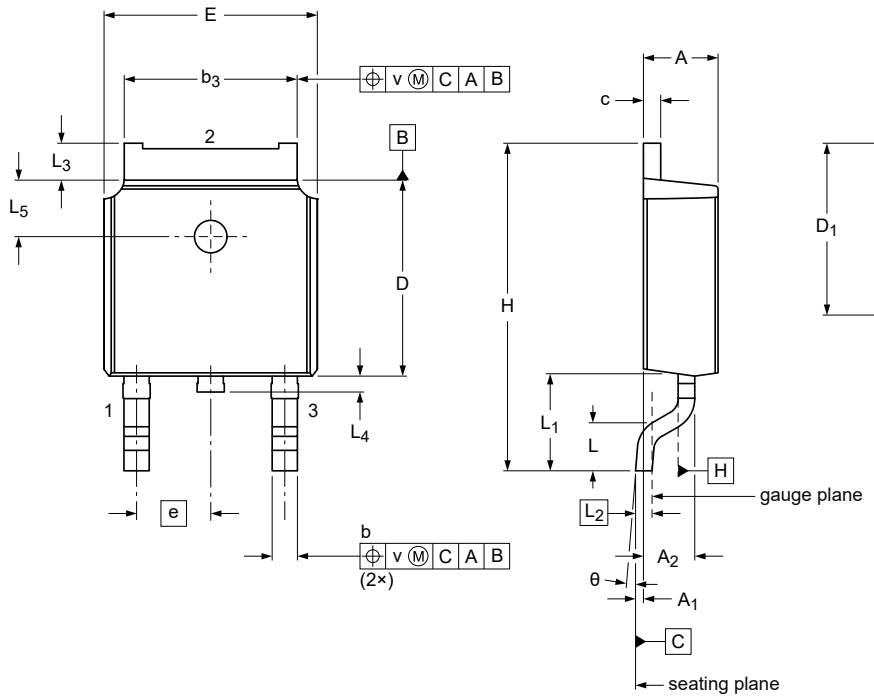


T_j = 125 °C

Fig. 26. Source current as a function of source-drain voltage; typical values

11. Package outline

plastic, single-ended surface-mounted package (DPAK); 3 leads;
2.286 mm pitch; 6.1 mm x 6.6 mm x 2.3 mm body **SOT428-2**



0 5 mm
scale

Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	b	b_3	c	D	D_1	E	E_1	e	H	L	(L_1)	L_2	L_3	L_4	L_5	v	θ
mm	max	2.40	0.13	1.17	0.90	5.46	0.61	6.22	5.30 REF	6.73	4.83 REF	2.286 BSC	10.50	1.75	2.90 REF	0.51 BSC	1.28	1.00	1.95	0.01	8°
	nom	2.30		1.07	0.78	5.33	0.53	6.10		6.60			10.10	1.50					1.80		
	min	2.20	0.00	0.92	0.63	5.10	0.43	5.98		6.40			9.40	1.38			0.88	0.50	1.65		0°

Note
1. Dimensions do not include plastic protrusions.
2. Package outline exclusive of metal burr dimensions.
3. Datums A and B to be determined at datum plane H.

sot428-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT428-2						24-11-19

Fig. 27. Package outline TO252 (SOT428-2)

12. Soldering

Footprint information for reflow soldering of TO252 package **SOT428-2**

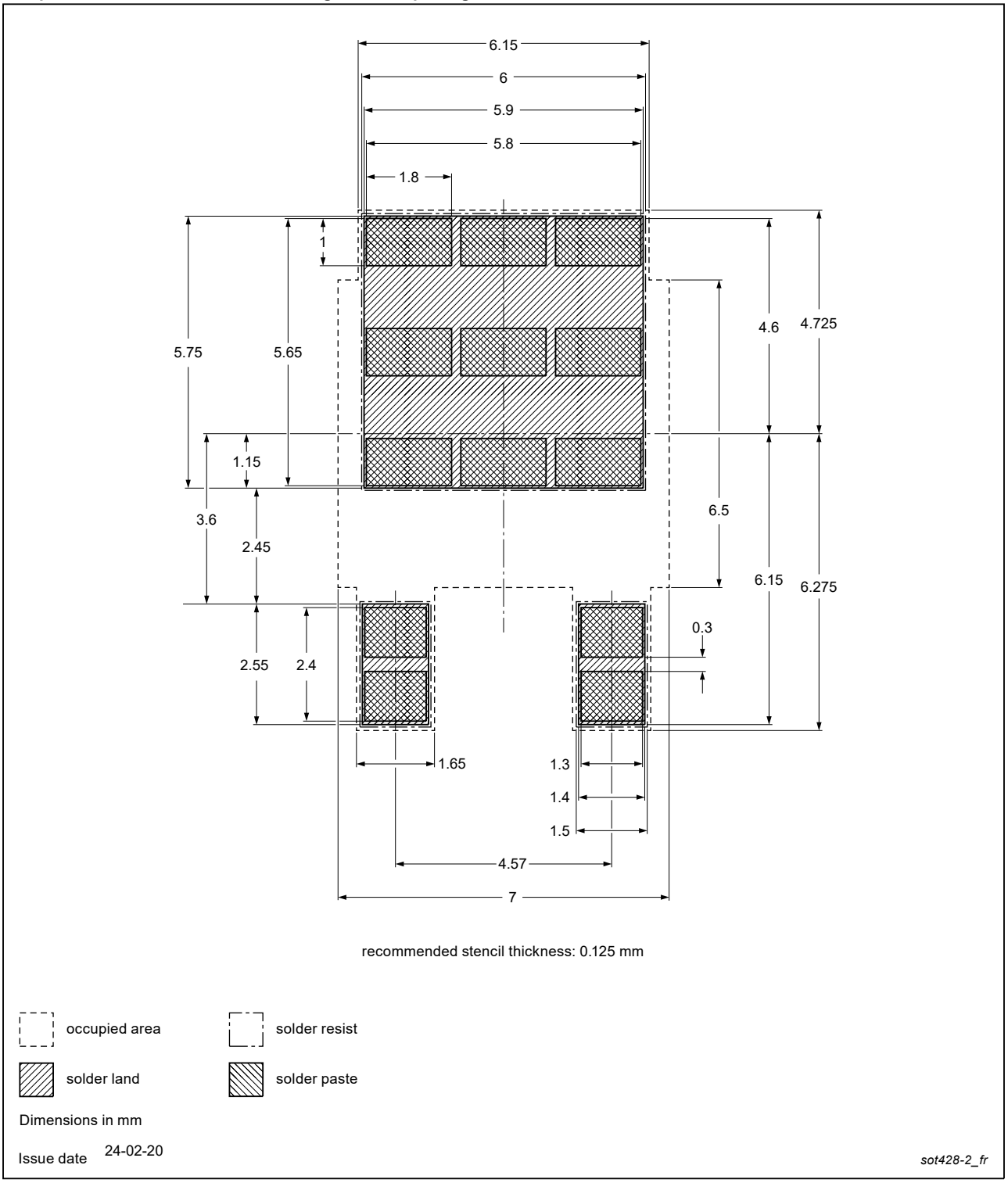


Fig. 28. Reflow soldering footprint for TO252 (SOT428-2)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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